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Design of 1-bit Full Adder using output wired CMOS Inverter based Threshold Gate

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***Abstract*—A new implementation technique of 1-bit Full Adder using output wired CMOS inverter based threshold logic is presented. With the advancement of nano technology threshold gate based logic design has got a new direction. In this paper first carry output is designed using output wired CMOS inverter based majority gate. Then Sum output is designed using Threshold gate. The number of transistor is less than the CMOS based Full Adder Circuit. The major advantage of this CMOS Threshold gate is it's simplicity. It's delay time is only around three inverter delays. The proposed design has been verified by means of simulation using PSPICE.**

Keywords— ***Adder; Threshold Logic (TL) Gates; Majority gate; Complementary Metal Oxide Semiconductor (CMOS).***

I.INTRODUCTION

In this paper we propose a novel full adder cell which is a key component in all kinds of computing systems. The adder cell is based on linear threshold logic and majority gate [1]. There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity and regularity and good driving ability [2]. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area [3, 4, 5].

In Integrated Circuits mainly two types of full adders (Static & dynamic) are used. Static full adders commonly are more reliable, simpler .In this paper a static design of Full Adder is proposed. Threshold logic (TL) was introduced over six decades ago. There are many theoretical results showing that TL circuits are more powerful than classical Boolean circuits. It also offers much larger fan-in in comparison with the conventional logic gates [6]. A logical function which is linearly separable can be designed using threshold logic. However different TL gate realizations are made in recent papers [7,8,9 10,11,12].

The remainder of this paper is organized as follows:

SectionII: Describes the concept of threshold logic.

Section III: Describes the concept of majority gate.

SectionIV: Describes output wired CMOS inverter based threshold and majority gate

SectionV: Investigates the output wired CMOS inverter based one bit Full-Adder and its output waveforms.

Section VI: Gives the conclusion of the whole experiment

II. The concept of Threshold Logic

A linear threshold gate (LTG) is an n binary input and one binary output function [13].

Threshold Logic Gates are able to compute any linearly separable Boolean function given by-

$$Y = \text{sgn}\{F(x)\} = \begin{cases} 0, & \text{if } F(x) < 0 \\ 1, & \text{if } F(x) \geq 0 \end{cases} \quad (1)$$

$$F(x) = \sum w_i x_i - \psi \quad (2)$$

Where x_i is the n Boolean inputs and w_i is the corresponding n integer weights. The LTG compares the weighted sum of inputs and the threshold value ψ. If the weighted sum of inputs is greater than or equal to the threshold, the gate produces logic 1. Otherwise, the output is logic 0.

The basic Boolean logic functions AND,OR,NAND,NOR and NOT can be represented in the form of (1) and (2) as follows:

$$\text{AND}(x1, x2) = \text{sgn}\{ x1 + x2 - 1.5\} \quad (3)$$

$$\text{OR}(x1, x2) = \text{sgn}\{ x1 + x2 - 0.5\} \quad (4)$$

$$\text{NAND}(x1, x2) = \text{sgn}\{- x1 - x2 + 1.5\} \quad (5)$$

$$\text{NOR}(x1, x2) = \text{sgn}\{- x1 - x2 + 0.5\} \quad (6)$$

$$\text{NOT}(x1) = \text{sgn}\{- x1 + 0.5\} \quad (7)$$

These basic logic functions can be designed with threshold gate as shown in figure 1.

In this diagram AND gate is designed. Other gates can be also designed by changing the weights and threshold values.

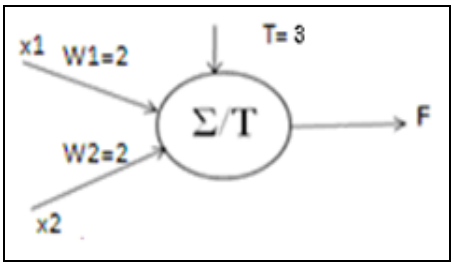


Figure 1: Design of Threshold logic based AND gate

III. The Concept of Majority Gate

The majority gate gives the logic output 1 when the number of one is more than the number of zeros at the input side. As for example OR gate is a Majority Gate. It is a special application of threshold logic. The majority gate can be designed using ganged output wired inverter circuit. [14]

IV. Output Wired CMOS Inverter Based Threshold and Majority Gate

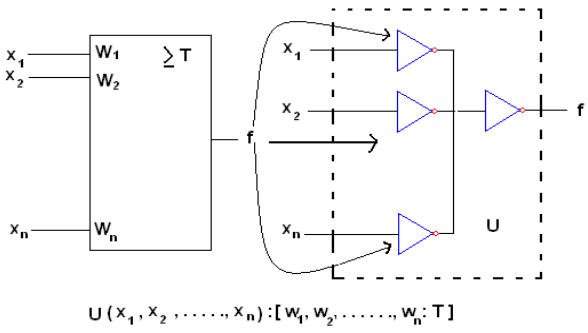


Figure2: Nonstandard symbol of Threshold gate and threshold gate basic structure using output wired ganged CMOS .

Figure 2 shows the nonstandard symbol for threshold gate and threshold gate basic structure using output wired ganged CMOS [15,16, 17]. Each input x_t drives one inverter, all inverter outputs are shorted together to design a nonlinear voltage divider which drives the output inverter whose purpose is to quantize the nonbinary signal at the ganged output node .The length of all the PMOS and NMOS transistors of inverters are same. The PMOS and NMOS transistor widths of each inverter are designed depending on the weight (W) and threshold value(T) to be implemented. The weight values other than 1 can be realized by changing the width of the PMOS transistor. Thus, the design process involves sizing only two inverters the basic input inverters and the output inverter.
A binary majority gate shown in fig3.

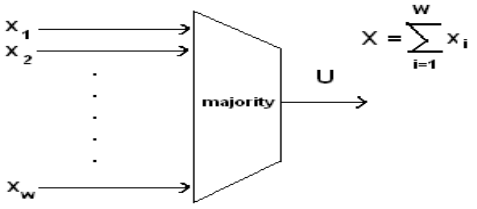


Figure 3: Function of majority gates

Here, w is the number of inputs which is usually odd. The output will be '1' if the number of '1's in the input side is more than the number of zeros.

A majority function is a special case of a threshold logic gate when the T is equal to (w+1)/2. The majority gate design based on ganged CMOS shown in Figure 4.

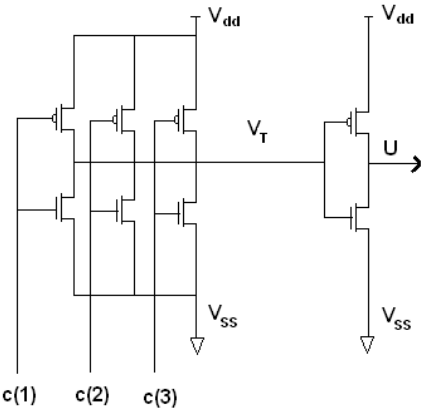


Figure4: Circuit of three input majority gate

It is made up of two parts: a nonlinear voltage divider made up of output wired inverters on the left hand side and an inverting buffer which senses the majority transition and provides a positive output on the right. The output inverting buffer isolates the divider output node from external circuitry to reduce noise effect and driving from the next stage. It also reshapes the output waveforms.

V. Design of One bit Full Adder using Output wired CMOS inverter based threshold AND MAJORITY gate

Here we have used one majority gate and one threshold gate to implement a full adder circuit. The threshold gate based implementation of full adder and the equivalent output wired ganged CMOS based one bit Full Adder circuit are shown in figure5 and figure 6. [18]

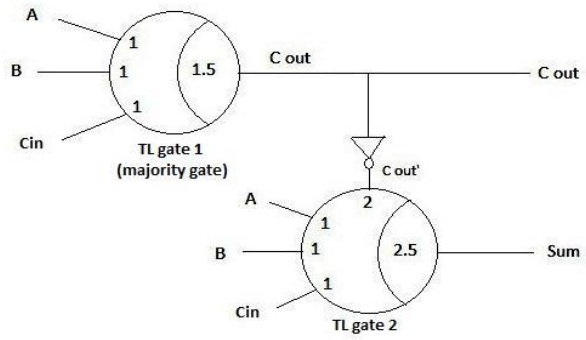


Figure5:Threshold Logic gate based Full Adder Circuit.

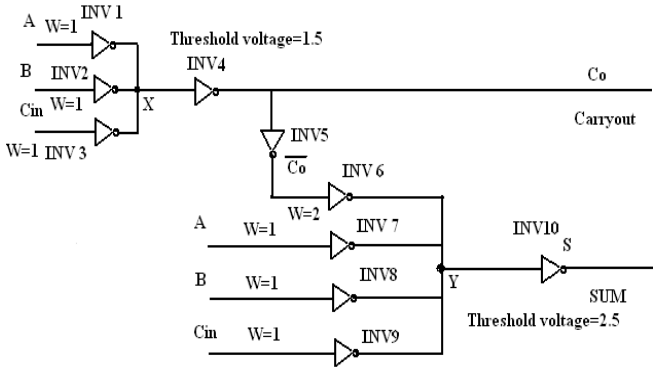


Figure 6: Output wired ganged CMOS based one bit Full Adder circuit

Here two threshold gates are used TL gate1 and TL gate2.TL gate1 gives the carry output and it is a majority gate.This Majority gate is designed using four inverters. Three of them are ganged and from that ganged output, the fourth inverter is connected to get the carry output. Inputs of full adder (A,B,Cin) are applied to three inverters(INV1,INV2,INV3) which is shown in figure 6. The W/L ratio of all the PMOS and NMOS transistors are chosen such that the resistance of all the transistors are equal (R).So The equivalent circuit of ganged part may be considered as a voltage divider network. Ganged output voltage at node X is calculated as a fraction of V_{dd} as shown in the following table.

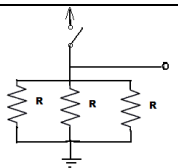
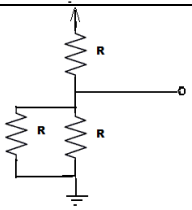
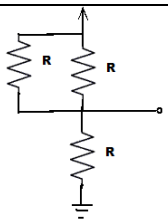
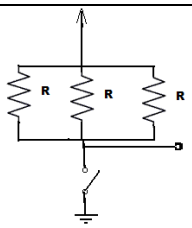
A	B	Cin	Ganged output voltage(Vx)	Equivalent voltage divider network
1	1	1	0	
1 1 0	1 0 1	0 1 1	Vdd/3	
1 0 0	0 1 0	0 0 1	2(Vdd/3)	
0	0	0	3 (Vdd/3)	

Table1:Ganged output voltage and its equivalent voltage divider network for different input combinations of majority gate(TL1).

According to this the threshold voltage of the last output inverter is set in between $V_{dd}/3$ and $2(V_{dd}/3)$. The last inverter gives the carry output.

Carry output is taken and inverted by another inverter(INV5). Ultimately this is used as a fourth input for the TL gate 2 which will give sum output.

INV6,INV7, INV8 and INV9 form the ganged CMOS for this threshold logic.For INV7,INV8,INV9 the weight is 1 so the resistances for PMOS and NMOS transistors of these inverters are same which is R. For Inverter6 the resistance of PMOS transistor will be R/2 which is adjusted by the W/L ratio of that transistor to achieve weight 2. The ganged output Voltage at node Y is calculated from the equivalent voltage divider network which is shown in the following table. The equivalent Voltage divider circuit is shown in figure7.

A	B	Cin	Co	Co'	Vy	S
0	0	0	0	1	3/4Vdd	0
0	0	1	0	1	1/2 Vdd	1
0	1	0	0	1	1/2 Vdd	1
0	1	1	1	0	3/5 Vdd	0
1	0	0	0	1	1/2 Vdd	1
1	0	1	1	0	3/5 Vdd	0
1	1	0	1	0	3/5 Vdd	0
1	1	1	1	0	2/5 Vdd	1

Table2: Ganged output voltage for TL2

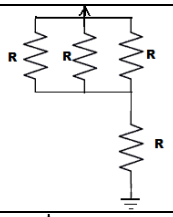
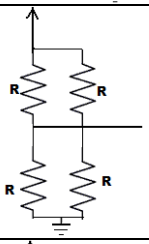
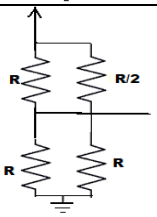
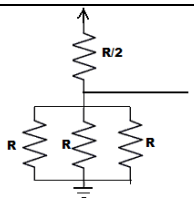
A	B	Cin	Co'	Equivalent voltage divider network
0	0	0	1	
0 0 1	0 1 0	1 0 0	1 1 1	
0 1 1	1 0 1	1 1 0	0 0 0	
1	1	1	0	

Figure7: Equivalent voltage divider network

From table 2 it can be concluded that the threshold voltage of the last inverter (INV10) should be in between 3/5 V_{dd} and 1/2 V_{dd}. According to this the last inverter is designed by adjusting the W/L ratio of the PMOS and NMOS transistors of it.

The circuit is simulated using PSPICE for 80ns.The 8 different input combinations exist for 10ns each. The supply voltage(V_{dd}) is taken as 3.3 V.The output waveforms are shown in figure 8.Upper one is for Sum output and lower one is for Carry Output.

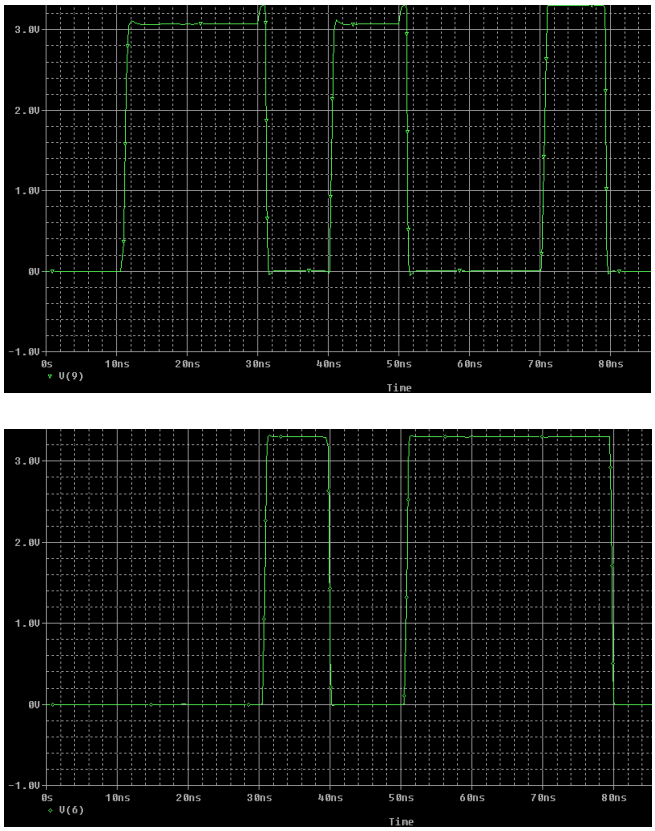


Figure 8: Sum and Carry output waveforms.

The total delay of the circuit is only five inverter delay which is almost 1ns measured for different models of transistor used.

VI.CONCLUSION

In this paper, we proposed the output wired CMOS inverter based one bit Full Adder circuit. The number of transistors required for this design is twenty.The total power consumption is 7.04E-04watts.

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