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DESIGN AND SIMULATION OF NOVEL TWO-STAGE OPERATIONAL TRANSCONDUCTANCE AMPLIFIER A USING FINFET

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Abstract—**In this paper novel two- stage operational transconductance amplifier (OTA) is designed using FinFET techniques & the responses are simulated. Basically design of OTA is totally based on MOS transistors that are essentially non linear which leads to deterioration The proposed circuit of two-stage OTA is used for low power consumption, increasing transconductance and efficiency of the circuit. Due to the operation of all the transistors in saturation region the output voltage is increased. By using proposed circuit the performance of two stages OTA is enhanced. Performance parameters for the designed circuit are as power consumption 38.13µW, gain margin 57.9dB, phase margin 104.31°, slew rate 30.76Vµ/sec etc. By introducing FinFET techniques the required power supply for the circuit decreases to 0.7V. Model parameters are calculated by using cadence virtuoso 6.1 in 45nm technology.**

Keywords: FinFET, CMOS Operational transconductance Amplifier (OTA), low power

I. INTRODUCTION

The Operational Tranconductance Amplifier (OTA) operates in differential input voltage and generates output current. OTA is an unbuffered op-amp and it produces high output resistance. Application for OTA includes voltage controlled low-pass or high-pass filters, waveform generators, amplifiers, modulators, comparators, and Schmitt triggers. OTA was designed in low power and frequency for the reduction in Transconductance in the circuit. Better noise optimization with good settling time is acquired using three-stage OTA design [1]. With different applications of OTA various techniques are being applied like single ended and rail to rail topology and performance parameter of the circuit is observed according to it [2]. Using feedback in the OTA design circuit better performance can be attained in the field of efficiency, Transconductance and output resistance of the circuit [3]. Higher gain-bandwidth product with lower supply voltage can be acquired using folded cascade topology and by removing the transmission gate from the circuit [4]. Slew Rate and leakage controlling can be obtained using Adaptive biasing technique in OTA [5].Controlling of Leakage reduction and better performance in current analysis can be obtained by using FinFET design [6]. High frequency and low power approach in OTA is used for higher tuning property and low current consumption in the circuit [7]. Higher gain and better transconductance can be obtained by designing OTA in 45 nm technology [8].

Better dimensionality and improved input offset voltage can be obtained using the Bulk degeneration technique [9]. OTA designed using two diode connected transistor in class AB amplifier led to achieve wide linear input range with high output performance at low supply voltage [10]. Designing of OTA at low power, low voltage and wide linear range in bulk-driven technique is shown as another method for designing of the circuit [11]. OTA circuit is simulated for high gain, high CMRR and low power consumption at low supply voltage and the performance of the circuit is observed [12]. Different values of Transconductance can be obtained with the variations in aspect ratio of transistor [13].

In this work, the advantages of the c Two stage OTA are considered to be carried out for a FinFET based two stage OTA circuit. The design is implemented with 45nm two stages OTA FinFET Technology and tested in Cadence virtuoso 6.1. The paper is summarized as follows, first is the introduction and working of operational transconductance

amplifier, then is the proposed circuit with performance parameter and comparison of proposed Two stage FinFET based OTA circuit with Two stage OTA circuit and simulation and result is compared by showing graph below.

II. OPERATIONAL TRANSCONDUCTANCE AMPLIFIER (OTA)

OTA is an electronic equipment is also process during which distinction of the two voltages because the input and current because the output. OTA may be a voltage controlled-current supply (VCCS). Since, voltage controlled-current supply is alleged that the output current (Io) is controlled by the input voltage (V1), the output current depends on the input voltage. The extra bias current (IB) is additional to controlled Transconductance. The operational transconductance amplifiers find wide application in the analog integrated circuit design. Because of high input impedance of the MOS devices the order for low-output impedance is not actual for the amplifiers which are inside integrated circuit. In this case only capacitive load presents at the output and accordingly high-impedance output stage with high voltage gain is suitable to use. The ideal model of OTA and equivalent circuit design is shown in fig. 1 and fig. 2 respectively.

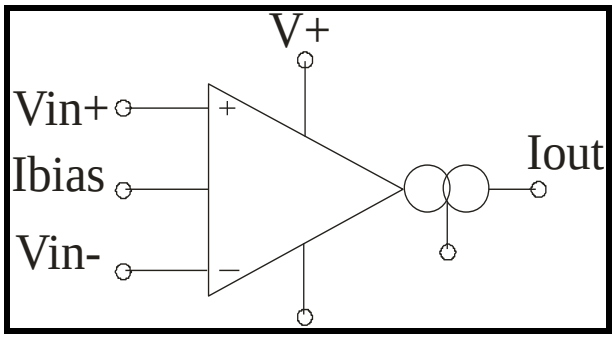


Fig 1: Symbol of OTA

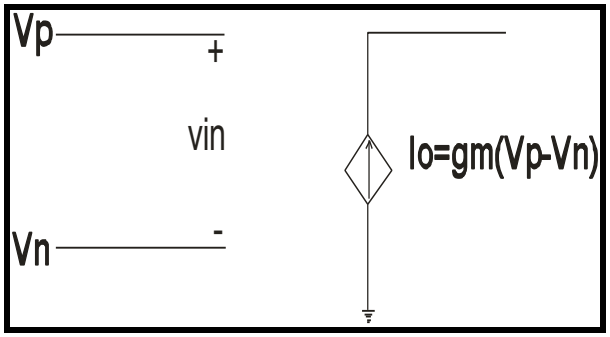


Fig 2: Equivalent circuit of OTA

Since the output of an OTA is current, the output impedance of the OTA is very high (ideally infinity). Since gm of the OTA is dependent on the *Ibis* current, the output of the OTA is controlled externally by the bias current (*Ibis*).

III. DESIGN PRINCIPLES

A. *CONVENTIONAL 2-STAGE OTA*

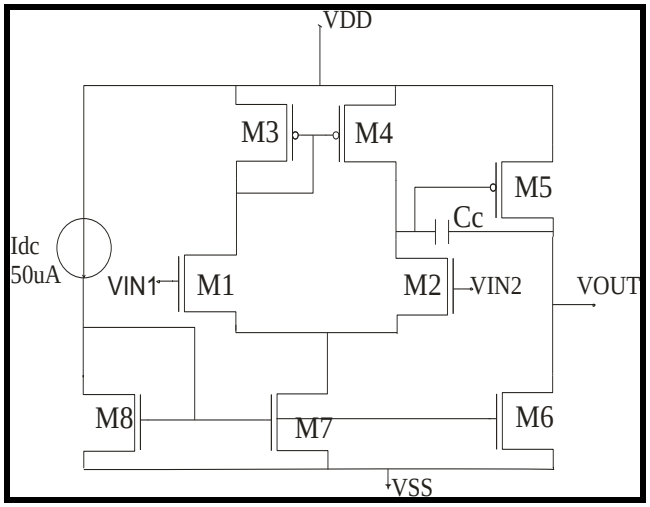


Fig.3. Conventional diagram of 2-Stage OTA

In VLSI technology the dimensions of CMOS decreases and power supply also reduces and speed of device is increase. So the OTA may be a basic building block in most of analog circuit with linear input-output characteristics also OTA is widely employed in analog circuit include such as Instrumentation amplifier with ADC and Filter circuit. The OTA is same as operational Amplifier in which having differential inputs.

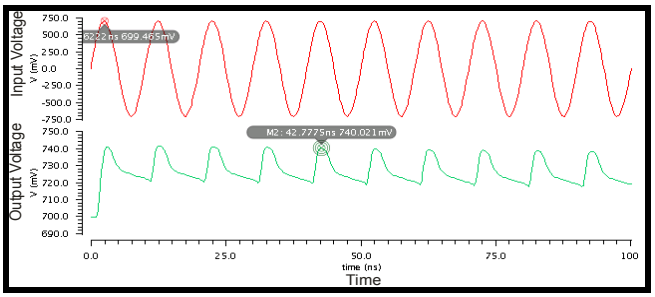


Fig.4. Output of Conventional 2-Stage OTA

$$R = r6 / r7 \qquad (1)$$

Where,

R=output resistance

r6 and r7= internal resistance

The ideal transfer characteristics are as follow:-

Mathematically expression,

Iout = gm (Vin+ − Vin−) **(2)**

Iout = gm * Vin **(3)**

Where,
Gm = Transconductance,
IC = control current,
Vin+ = Non inverting
Vin- = Inverting
Vin is input voltages.

B. PROPOSED CIRCUIT OF 2-STAGE OTA

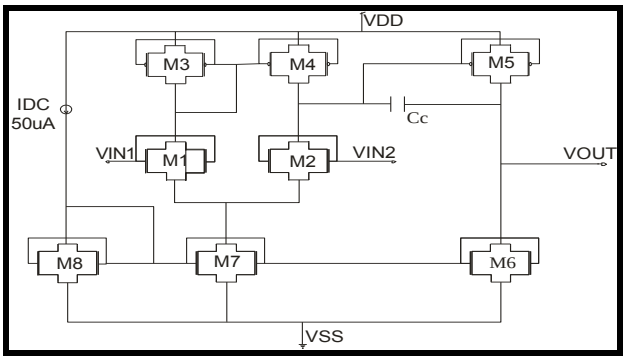


Fig.5.Proposed diagram of Two-stage OTA by FinFET Technique

FinFET is stand for 'fin-Shaped Field Effect Transistor' which describes a non planar, double transister built on an SOI substrate, based on single gate transistor design. The important characteristics of FinFET is that conducting channel is wrapped by a thin si 'fin', which forms of the body of a device. The thickness of the fin determines the effective channel length of the devices. In terms of its structure, it typically has a vertical fin on a substrate which runs between a larger drain and source area. This protrudes vertically above the substrate as a fin. The gate orientation is at right angles to the vertical fin. And to traverse from one side of the fin to the other it wraps over the fin, enabling it to interface with three side of the fin or channel. This form of gate structure provides improved electrical control over the channel conduction and it helps reduce leakage current levels and overcomes some other short-channel effects.The term FinFET is used somewhat generically. Sometimes it is used to describe any fin-based, multigate transistor architecture regardless of number of gates. Since, a design of a proposed OTA with 45nm FinFET technology is proposed and shown in fig. 5 above.

WORKING:

The two stage OTA architecture consists of two stages. Its configuration is similar to the considered operational voltage amplifier Op Amp. The first stage is a differential amplifier (M1, M2, M7) with current mirror load (M3, M4). It ensures high value of the CMRR. The second stage is a common source amplifier with active load (M5, M6). Transistor M8 is for the biasing of M8-M7 and M8-M6 current mirrors. Iref is a constant current reference. As we know from previous modules, transistors M1 and M2, and M3 and M4 are identical. Also the Miller capacitance Cc is introduced, in order to guarantee the stability of the circuit.

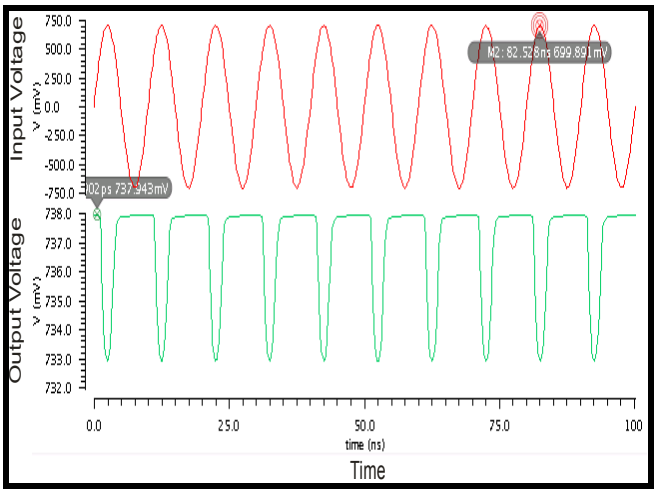


Fig.6. Output of Proposed 2-Stage OTA

IV. OTA PRACTICAL CONSIDERATION

(A).Noise

Noise may be define that random fluctuation in all electrical and electronic circuits Or in alternative, word noise is unwanted signal that arises by environment like natural and man-made artificial sources like vehicle and a few electronic equipment.

$$Sv(f) = 4kTR, \quad f \geq 0 \qquad \textbf{(1)}$$

Where,
k= Boltzmann constant
R= noiseless resistor
T= temperature

(B).*Voltage Gain*

Voltage may be defined, in which circuit of the gain is improving in the power factor of output to input. Quantitative relation of voltage measured at the output to voltage measured at the input. Calculation of the voltage gain is observed in logarithmic scale in decibel.

$$A_u = \frac{v_{out}}{v_{id}} = \frac{i_o r_{out}}{v_{id}} = \frac{i_o}{v_{id}} r_{out} = G_m r_{out} = \frac{g_{m5} \cdot g_{m2}}{(g_{o5} + g_{o6})(g_{o2} + g_{o4})}. \qquad \textbf{(2)}$$

$$Voltage\ Gain = 10 \log \left(\frac{Vout}{Vin}\right) dB \quad \textbf{(3)}$$

Vout= Output Voltage.

Vin = Input Voltage.

(C).Phase Margin

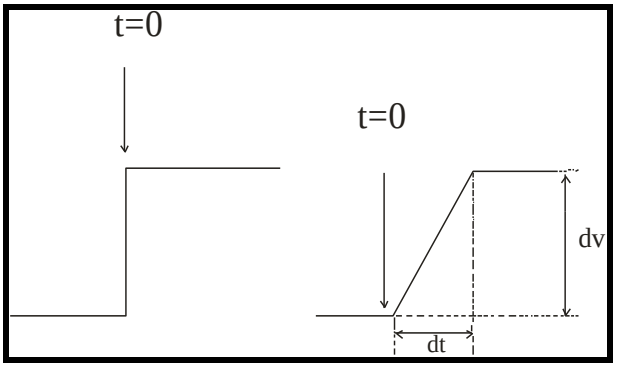
Phase margin is nothing but, in electronic equipment the difference between the phases is calculated in degree and 180º also and amplified output signal is a function of frequency. One's the loop gain is 1.0 the phase margin is the difference between response of phase or -180º.Phase margin is also said that the negative phase perturbation by which system is marginally stable.

$$P.M. = 180º + \angle\ G(jWgc) \quad \textbf{(4)}$$

Where,
gc = gain crossover frequency

(D).Slew Rate

The rate of change of the closed-loop amplifier output voltage for a signal input. The pulse is faster at slew rate is low. Since, pulse can change its state for higher output performance the slew rate is mostly determined by the utmost current obtainable to charge or discharge capacitance. It unit is v/µs.



$$\text{Slew Rate} = \frac{\Delta \text{Vout}}{\Delta \text{t}} \quad \textbf{(5)}$$

Where
$\Delta Vout$ = Voltage at Output
Δt = time

(E).Power Consumption

To achieving power consumption dimension is vital in all CMOS based circuits In CMOS based circuit short channel effect is arise, to overcome this effect we used FinFET techniques. In some other, word what proportion power is consumed by the circuit by which we have tendency to get desired output. Power consumption is measured in kilowatt hours (kWh).

$$\text{Power (P)} = (\text{Vdd}) * (\text{Iavg}) \quad \textbf{(6)}$$

Where,
Vdd = supply voltage
Iavg = average current.

(F). Gain Margin

The reciprocal of the open-loop voltage amplification at the lowest frequency at which the open-loop phase shift is such that the output is in phase with the inverting input the gain margin is nothing however within which the problem by that the gain |G(jw)| has got to be magnified for operational transconductance amplifier. The expression of gain margin is in dB. The gain margin defines as follow**:**

$$GM = |G(j\omega 180^\circ)| - 1 \quad \textbf{(7)}$$

$$\text{GM} = -1/\text{G(jWpc)} \quad \textbf{(8)}$$

Where,
ω180◦ is such that G(jω180◦) = 180◦.
pc = phase crossover frequency

(G). *Efficiency*

Efficiency of a circuit is that the ability of providing the higher output power once any input is provided within the circuit. It's the foremost vital parameter within the analog circuit. It is defined as the ratio of the output power obtained from the circuit to the input power provided to the circuit. It's calculated in proportion (%).

$$\eta = \frac{\text{Pout}}{\text{Pin}} \quad \textbf{(9)}$$

Where,

Pout = Output power is measured.

Pin= Input power is measured.

(H).*Transconductance*

The circuit performance is ascertained by measuring Transconductance. The circuit is good as much as transconductance is more. It is defined as the ratio of the change in output current to the change in input voltage terminal. It is denoted by gm.

$$gm = \left(\frac{\Delta Iout}{\Delta Vin}\right) \quad \textbf{(10)}$$

Where,

$\Delta Iout$ = Current at output terminal

ΔVin = Voltage at input terminal

(I). *Gain-Bandwidth product*

The frequency, at which the gain starts decreasing is called the bandwidth **BW** or the **−3dB** frequency. The product of the low-frequency gain and the bandwidth is called the Gain-Bandwidth product **GBW**. Its value is much closed to unity gain frequency **fu** - the frequency, at which the gain is equal to 1 (0dB).

$$GBW = \frac{g_{m1}}{2\pi C_c}; \quad SR = \frac{I}{C_c}, \; where \; I = \min(I_{D5}, I_{D7}). \qquad \textbf{(11)}$$

V. SIMULATION AND RESULTS

A. SIMULATION

1. During this FinFET technique that we tend to employed in this paper we've got seen a reduce in noise and therefore the noise curve as shown in fig. 6.

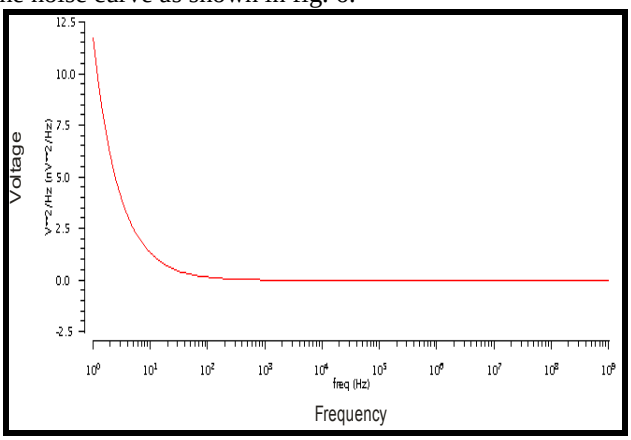


Fig.7. Noise

2. During this paper we seen a reduction in power consumption by using FinFET technique, it is best for circuits as shown in fig. 7

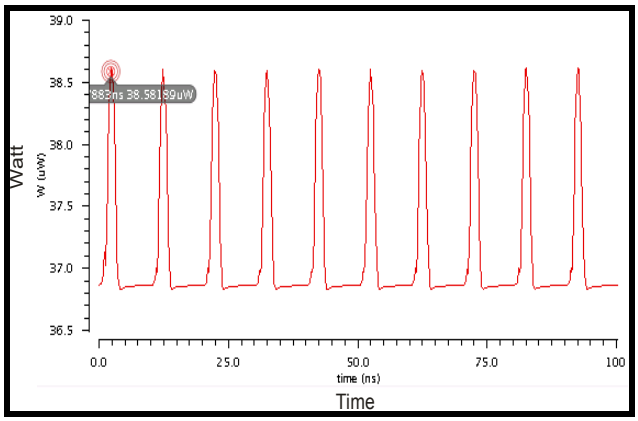


Fig.8. Power Consumption

3. Phase Margin and Gain Margin of 2-stage OTA

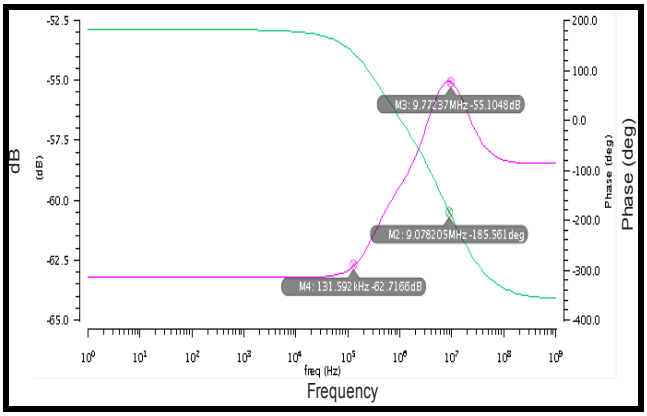


Fig.9. Phase Margin and Gain Margin

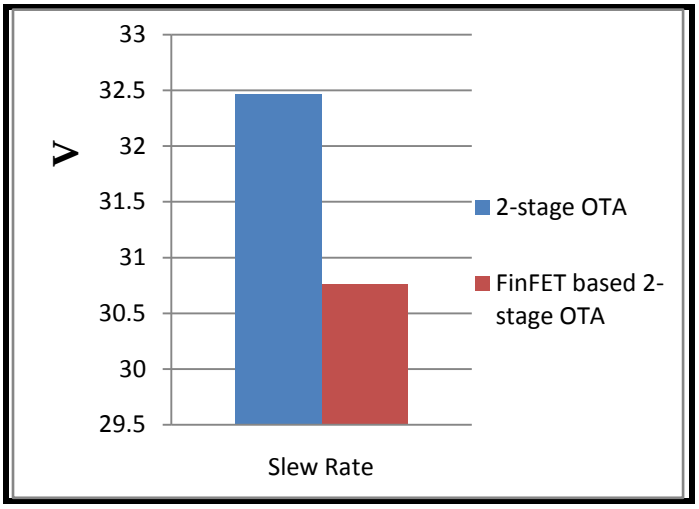
B. RESULTS

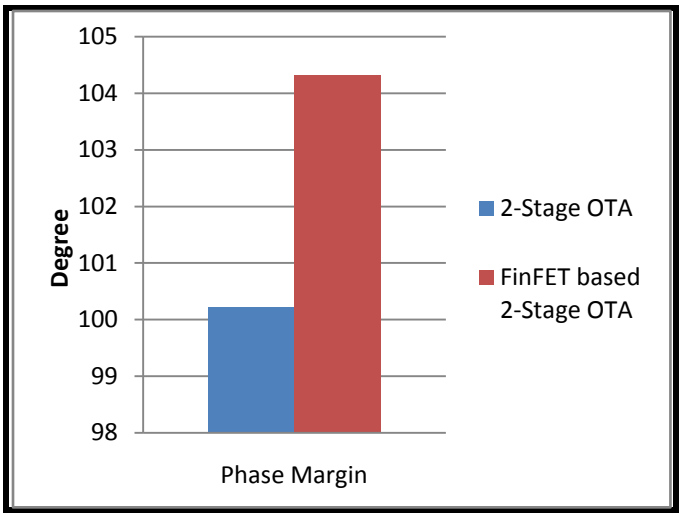
Table 1: Comparison table for Two-Stage OTA and FinFET based Two-Stage OTA

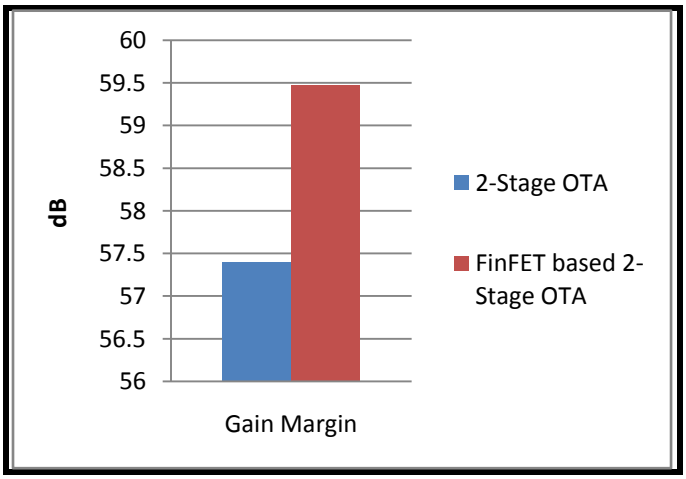
Sl. No	Parameters	Two-Stage OTA	FinFET based Two-Stage OTA
1	Noise(V2/Hz)	3.56954E-14	2.45732E-17
2	Power Consumption (µW)	41.99	38.13
3	Supply voltage(V)	0.7	0.7
4	Slew Rate	32.47	30.76
5	Leakage Power	45.45E-9	39.22E-12
6	Phase margin	100.21°	104.31°
7	Gain	57.4	59.47

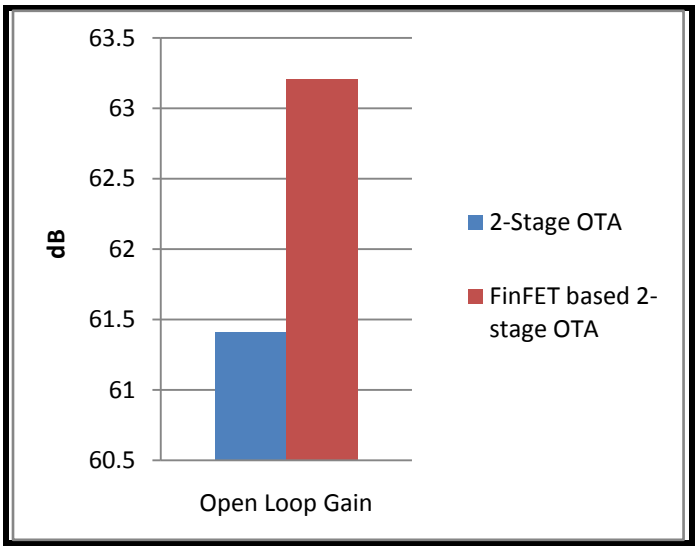
	margin(dB)		
8	Open loop gain(dB)	61.41	63.21
9	Transconductance	1.5779E-6	2.221E-4
10	Voltage Gain	30.7dB	31dB

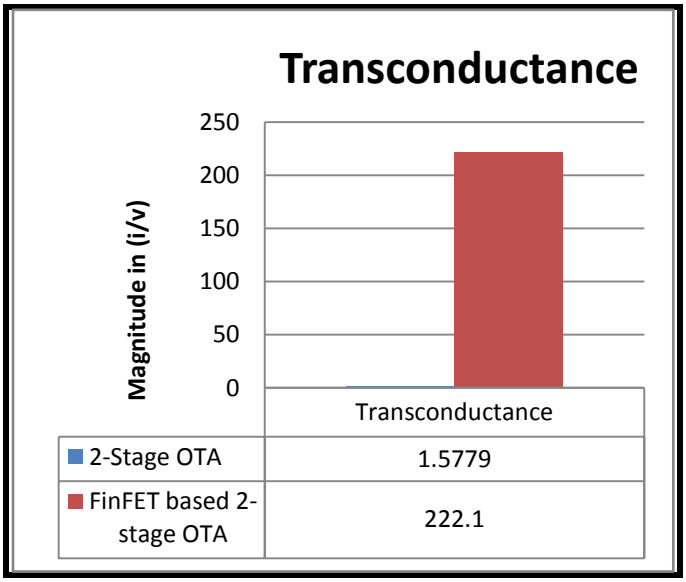
Tabular representation of the compared data is given above table.1. From the above mentioned data the graphical comparison is done. As we can see that all the parameters calculated have decreased and performance of the device is enhanced by using the proposed novel FinFET technique in place of CMOS.

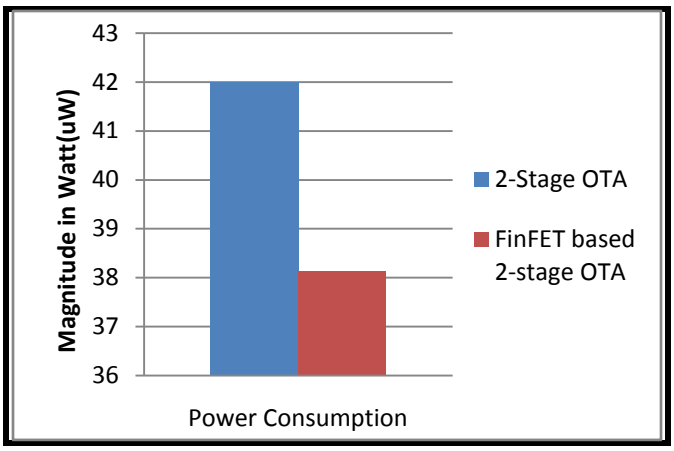












VI. CONCULSION

In this, paper Two stage OTA is optimized and result is simulated in 45nm technology. By exploitation, FinFET in place of two-stage OTA there is reduction in the gain margin59.47dB, phase margin104.31º, power consumption38.13mW and slew rate 38.13 V/µs etc. By exploitation FinFET technique power consumption is obtained is 41.99 mW from 38.13 mW. In my simulation result power dissipation, phase margin, gain margin, voltage gain employed good result.

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REFERENCES

[1] Siddharth Seth and Boris Murmann ., "Settling Time and Noise Optimization of a Three-Stage Operational Transconductance Amplifier" IEEE transactions on circuits and systems, vol. 60, no. 5, May 2013

[2] M. F. Li, Uday Dasgupta, X. W. Zhang, and Yong Ching Lim," A Low-Voltage CMOS OTA with Rail-to-Rail Differential Input Range", IEEE Transactions on circuits and systems, Vol. 47, pp. 1, January 2000

[3] Shanshan Dai, Xiaofei Cao, Ting Yi, Allyn E. Hubbard, and Zhiliang Hong," 1-V Low-Power Programmable Rail-to-Rail Operational Amplifier With Improved Transconductance Feedback Technique",IEEE Transactions on very large scale integration (vlsi) systems, Vol. 21,pp. 1928-1935, September 2013

[4]. Fabian Henrici, Joachim Becker, Maurits Ortmanns, Yiannos Manoli," A Switchable Folded-Cascode OTA without Transmission Gates in the Signal Path", IEEE Conference, pp.180-183, November 2008.

[5]. Fabian Henrici, Joachim Becker, Maurits Ortmanns, Yiannos Manoli," A Switchable Folded-Cascode OTA without Transmission Gates in the Signal Path", IEEE Conference, pp.180-183, November 2008.

[6]. Zehan Kesilmiş, Mutlu Avc, Murat Aksoy3," An operational Transconductance amplifier with 45nm finfet technology ", 2011

[7]. Dmitry V. Morozov and Alexander S. Korotkov, "Transconductance Amplifier With Low-Power Consumption", IEEE Transactions on circuits and systems, Vol.52, pp. 11, November 2005

[8]. Navneet Dubey and Shyam Akashe"Low Power Two-Stage Operational Amplifier design using 45 nm Technology", International Journal of Modern Engineering & Management Research(IJMEMR) , Vol.2, pp. 15-20, December 2014

[9]. Joel Gak, Matías R. Miguez, and Alfredo Arnaud, "Nanopower OTAs with Improved Linearity and Low Input Offset Using Bulk Degeneration" IEEE Transactions on circuits and systems, Vol. 61, pp. 03, March 2014

[10] A. Yodtean, "A CMOS OTA and Implementation," IEEE International Symposium on Intelligent Signal Processing Communication Systems (ISPACS) , pp. 1-4, 2014

[12] S. Goswami, "Analysis and Design of Two-Stage Operational Transconductance Amplifier," vol. 2, no. 4, pp. 9–14, 2014

[13] Abhay Pratap Singh, Sunil Kr. Pandey, Manish Kumar," Operational Transconductance Amplifier for Low Frequency Application" International Journal of Computer Technology and Applications (IJCTA), Vol. 3, pp. 1064 -1066, May-June 2012