American Journal of Electronics & Communication

Ankit Singh Kushwah et al, American Journal of Electronics & Communication, Vol. I (1), 19-24

Design and Analysis of Magnetic Tunnel Junction Based Random Access Memory Cell

Ankit Singh Kushwah
Department of ECE
Institute of Technology and Management
Gwalior, India
akushwah13@gmail.com

Shyam Akashe
Department of ECE
ITM University
Gwalior, India
shyam.akashe@itmuniversity.ac.in

***Abstract*— In this report, we presented an NV Random Access Memory cell using a novel easy and proficient model of Spin Transfer Torque Magnetic Tunnel Junction (STT-MTJ). Magnetic tunnel junction (MTJ) devices are CMOS well suited with high steadiness, high dependability and non-volatility. The combination of magnetic tunnel junction with CMOS circuits in magnetic RAM (MRAM) or Magnetic FPGA can get the digital circuits to major advantages related with non-volatile facility like immediate on/off, Zero standby power use of goods and services. MTJ (Magnetic Tunnel Junction) devices have various advantages over other magneto-resistive devices for use in MRAM cells, like MRAM produces a big signal for the read operation and a varying resistance that can make the circuit. Due to these attributes, MTJ-MRAM can operate at high velocity. A completed simulation model for the 5T and 2MTJ SRAM design is shown in this report, which is grounded on the recently confirmed STT (Spin-Transfer Torque) writing technique which promises to take down the switching current losing to ~150µA and the STT RAM cache reduces total power consumption from 44.6µW -13.2µW. This model has been confirmed in Verilog A language and the whole work carried out and ran out on cadence virtuoso platform at 45nm.**

***Keywords*— Non-volatile; STT-MTJ; MRAM; High speed; Magnetic logic.**

I. INTRODUCTION

Withering of the complementary metal-oxide semiconductor (CMOS) fabricated node below 90nm, the high supply power due to rising leakage currents becomes a more and more significant subject. This upgrade power use of static random access memory (SRAM) based low rank cache memory shows the harshest problem in superior processor particularly used for battery used computing devices. To master these problems a quantity of non-volatile storage technologies such as Magnetic RAM (MRAM), Ferroelectric RAM (FRAM), Phase-Change RAM (PCRAM) and Resistive RAM etc. are under examination. These devices are expected to over the above problem in the CMOS logic circuit and take the non-volatility into the CMOS logic circuit and permit them to completely power OFF. All the data are confined and can be retrieved immediately on Active state. This technique could overcome the standby power issue and allow the

Circuits and technology to be further shrunk down. MTJ (Magnetic Tunnel Junction) is considered as one of the most hopeful rising technologies to overcome the high leakage power issue of CMOS circuits and MTJ circuit also provide non volatility unbounded endurance and fast random access. In Magnetic Tunnel Junction it is one of the most gifted storage technologies, that features non volatility, high read/write speed, large withholding up to 10 years and it permits also more than 10^{12} reprogramming cycles.

A. MOTIVATION FOR STT-RAM

Presently, three cases of memory exist, Static RAM (SRAM), Dynamic RAM (DRAM), and Flash memory. SRAM has superb read and write speeds, but holds a very large cell size (requiring 6 or more transistors per cell). The speed of SRAM makes it rather suited for embedded applications, particularly cache memory, where execution is key than memory density. SRAM is volatile, but takes

very little active power for data retention. DRAM is able to offer much better storage density through its function of a single transistor with a storage capacitance. Even so, the capacitor leak off the charge and refresh the cycle after every few milliseconds. DRAM is typically used as the primary memory system in a computer, where memory density and public presentation are more significant in comparison to power using up. Flash memory technologies for fluid applications in which high volatility and very high densities are required. While Flash does have reasonably quick read access times, but very slow write speeds and endurance rates are really low (< 100,000 cycles). To sustain the power, performance and control the effectiveness of cost we use a typical organization that incorporates all the advantages of SRAM, DRAM and Flash memory called Magneto resistive RAM. Such a memory would reduces the need of multiple applications definite memories, and getting better system performance and reliability, while also reducing costs and power use of goods and services. MRAM based on the idea of way of magnetization to store binary information and exploit magneto resistive properties to retrieve the data [8].

TABLE I. COMPARISION OF MEMORY TECHNOLOGIES

	SRAM	***DRAM***	***FLASH (NOR)***	***FLASH (NAND)***	***STT-MRAM***
Non-Volatile	NO	NO	YES	YES	YES
Read Time (ns)	1-100	30-100	10	50	2-20
Write Time (ns)	1-100	15	1µs/1ms	1ms/0.1ms	2-20
Cell Size	50-120	6-10	10	5	6-20

II. MTJ TECHNOLOGY

MTJ circuits can be switch generally in three modes: field induced magnetization switching (FIMS), thermally assisted switching (TAS) and spin torque transfer (STT). FIMS is used in the first generation of MRAM, which was successfully commercialized. However, the high switching power expenses, large switching area, and bad cell selection performance of the conventional MRAM writing approach Field-Induced Magnetic Switching (FIMS) is not good with future respect. And in other side another switching approach, Thermally Assisted Switching (TAS) -MRAM promises to lower the reconfiguration latency and enhance the writing selectivity, but it is also not good for future because decrease the chip area and programming power due to the comparatively high switching current and the heating current. To overwhelm all these drawbacks of FIMS and TAS technologies we developed a novel technology called STT RAM [4].

TABLE II. COMPARISION OF STT-MTJ TECHNOLOGIES

MTJ Device	***SPEED***	***AREA***	***POWER***
FIMS-MTJ	High	Large	Very High
TAS-MTJ	Medium	Medium	Medium
STT-MTJ	High	Small	Low

A. Spin Transfer Torque MTJ

In MTJ (magnetic tunnel junction) it have two ferromagnetic layers and one oxide barrier layer, e.g., MgO. The resistance of MTJ can be judge by the magnetization information of ferromagnetic layer with spin direction: when the direction of magnetization of spin is parallel (anti-parallel), MTJ is in low (high) resistance state. In STT-RAM design, the magnetization order of one ferromagnetic layer (reference layer) is developed by matching to a pinned magnetization layer while the magnetization order of the other ferromagnetic layer (free layer) can be altered by going across a switching current polarized by the magnetization of the reference layer [10].

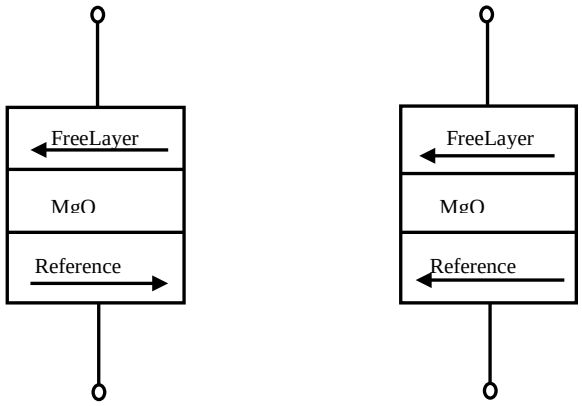


Fig. 1. MTJ Structure (a) Anti-Parallel (high resistance state). (b) Parallel (low resistance state).

The value taken as ‘1’ if the directions of layers are parallel and MTJ shows low resistance and a ‘0’ if the direction read as anti-parallel and MTJ shows high resistance or vice versa for negative sense. The MTJ shows low resistance when the two layers (free layer and reference layer) are magnetized in the same and it offers high impedance when the direction of magnetization of both the layers is opposite, named the “ant parallel state”. Figure shows the states of an MTJ in high resistance mode or low resistance mode. In MRAM cell an NMOS transistor is added to form a NMOS as a read transistor in series with the MTJ. Fig.2, bit-line linked to the bit cells as bit-line (BL), source-line (SL) and word-line (WL). The data is read as ‘1’ if the MTJ shows low impedance and a ‘0’ if the MTJ shows high impedance or vice versa for negative logic.

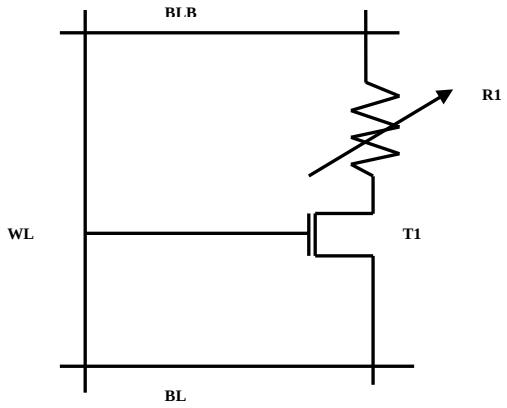


Fig. 2. 1T 1R STT-MRAM cell structure

The memory component in an STT-MRAM cell is a magnetic tunnel junction (MTJ), It is used as a variable resistance. A characteristic single-transistor-one-resistor (1T1R) STT-MRAM cell is presented in Figure 1. The access transistor is in serial publication with the MTJ. To scan the cell, the word line (WL) makes high and the impedance of the MTJ is determined. To write the cell, the word line makes high and the cell is forced by a write current. The centring of the write current determines the value of the bit written to the cubicle.

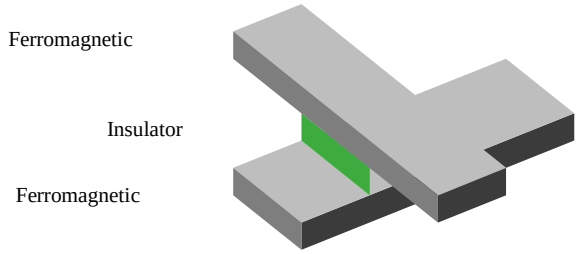


Fig. 3 Basic structure of an MTJ

III. 5T-2MTJ BASED NV-SRAM CELL

To overcome the difficulties of non-volatility in planar CMOS transistor based SRAM uses a new style of the 4T-2MTJ based SRAM cell, in which MTJ (Magnetic Tunnel Junction) is a variable resistance whose equivalent circuit shown above in figure (3). MTJ switches in two modes, (1) Parallel mode (low impedance state) and (2) anti-parallel fashion (high impedance state). The information is read as '1' if the MTJ offers low impedance and a '0' if the MTJ offers a high resistance or vice versa for negative logic. The Schematic of 5T-2MTJ based SRAM cell shown below.

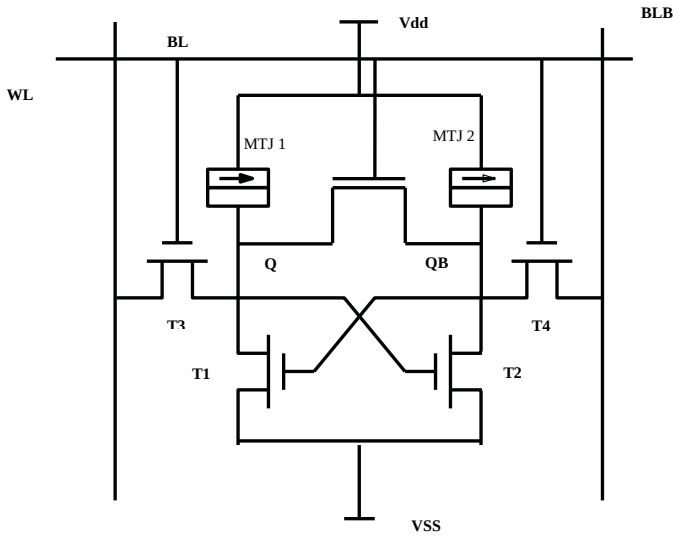


Fig. 4. 5T-2MTJ NV-SRAM

A. Non-volatile SRAM modes of operation

Non-Volatile SRAM cell shows the following basic ways of functioning:

Data retention or Standby mode: An SRAM cell is capable to hold the information indefinitely.

- Read mode: An SRAM cell is capable to exchange its stored information. This procedure does not impress the data, i.e., read operation is non-destructive as compared to DRAM's read operation.
- Write mode: The records of an SRAM cell can be arrange to any binary value, disregarding of its original stored value.
- Cell Operation: We can carry out both read or write operation on the mobile phone. For write operations two signals will be produced from the input data one is 'BL' and another is 'BLB'. Where BL = data and BLB = complement of information. Then word line (WL) goes high which makes on the operational transistors and the information will be penned in the cubicle. For a read operation both 'Bit Line' and 'Bit Line Bar' lines are pre-charged to voltage level "v" and then 'Word Line' goes high, since SRAM has been already either in state '0' or in '1', then, granting to the nation only one line discharges to Ground and a voltage difference developed between 'Bit Line' and 'Bit Line Bar' lines. This conflict will be sensed by sense amplifier and at last stored bit will be available at the output of sense amplifier.

IV. POWER CONSUMPTION

The total power of the circuit results the power dissipation across entire circuit. And it can state as:-

$$P_{total} = P_{dyn} + P_{static} \quad (1)$$

P_{dyn} represents dynamic power dissipation through capacitance due to charging/discharging when a transition makes occur through the output signal of a logic gate. P_{static} is the static power consumption which occurs due to the leakage current whose major elements are the sub threshold leakage, gate direct tunnelling leakage, and junction band-to-band tunnelling leakage [8].

In general it express as

$$P = I * V \quad (2)$$

Power using up in any digital integrated circuit, is afforded by the equation

$$P_{total} = I_o V + \alpha C V^2_{dd} f \quad (3)$$

Where, I_o is the leakage current, which is regulated by the diode equation $I_s (e^{qv/kT} - 1)$, V_{dd} is the power supply voltage, α shows the characteristic of average switching activity factor, The total capacitance of the circuit represents by C, and f shows the frequency of operation. The first term of the equation shows the leakage power and the second term shows the dynamic switching power. With the reduction in features sizes, Vdd has also fallen and the threshold voltage V_t of the transistor trying to reduce. So the leakage current Io, which depends on V_t, given by diode equation increases [9]. A more detail expression for sub threshold leakage [11].

$$Isub = A * exp\left(\frac{q}{n' KT}(Vg - Vs - Vtho - \gamma Vs + \eta Vds)\right) * B \quad (4)$$

$$\text{Where, } A = \mu\, Cox \frac{Weff}{Leff}\left(\frac{KT}{q}\right)^2 e^{1.8} \quad (5)$$

$$B = 1\text{- } exp\left(\frac{-qvds}{KT}\right) \quad (6)$$

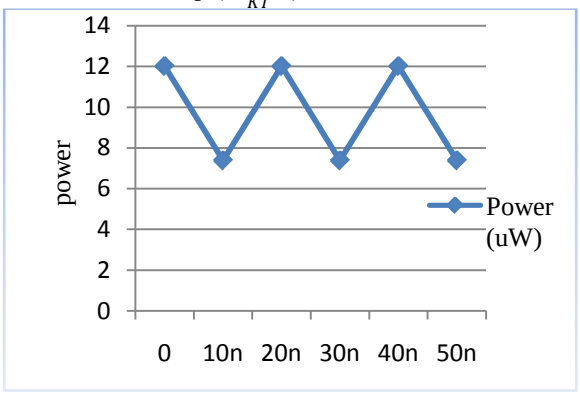


Fig. 5. Power consumption graph

V. CELL DELAY

The propagation delay times τPHL and τPLH can be evaluated by the input-to-output signal delay during the high-to-low and low-to-high transitions of the signal, respectively. In which, τPHL is the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage. Similarly, τPLH is defined as the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage. To analysis and calculate the derivation of delay expressions, the input voltage waveform is generally understood to be an ideal step pulse with zero rise and fall times. Under this assumption, τPHL becomes the time required for the output voltage to fall from VOH to the $V_{50\%}$ level and τPLH becomes the time required for the output voltage to rise from VOL to $V_{50\%}$ level [13]. The voltage at point $V_{50\%}$ level defined as follows:-

$$V_{50\%} = VOL + \frac{1}{2}(VOH - VOL) = \frac{1}{2}(VOH + VOL) \quad (7)$$

The average propagation delay τp of the inverter shows the average time taken for the input signal to distribute through the inverter.

$$Tp = \frac{\tau PHL + \tau PLH}{2} \quad (8)$$

TABLE II. COMPARISION OF DELAY

Parameter	*5T-2R SRAM*	*5T-2MTJ RAM*
Delay	21.54 E-9	20.34 E-9

VI. STATIC NOISE MARGIN (SNM) MEASUREMENT

The static noise margin (SNM) of SRAM cell is put as the minimum DC noise voltage required to throw the cell state.e. SNM of an SRAM cell is a widely-used intends metric that evaluates the cell stability. The measured results when plotted are called "butterfly curve". The butterfly curve can obtain by the following technique with the test circuit: 1) Word line (WL) is biased at the ground and bit lines (BL, BLB) are biased at VDD. 2) The voltage of N1 is change from 0 V to VDD while measuring voltage of QB. 3) The voltage of N2 is changes from 0 V to VDD while measuring voltage of Q in the same path. 4) Now calculated voltages are plotting to obtain a butterfly curve [12].

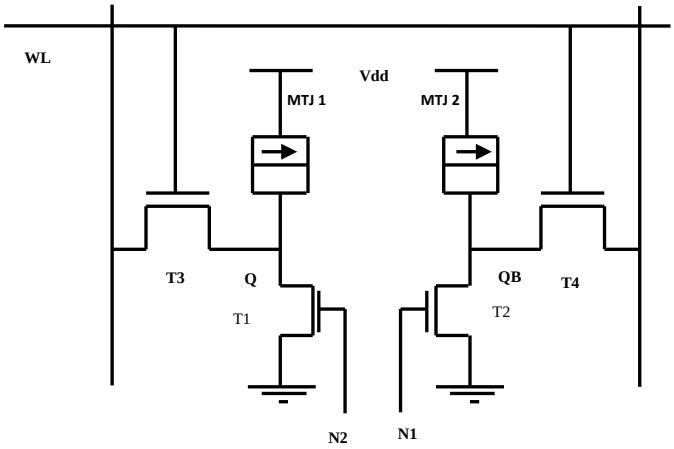
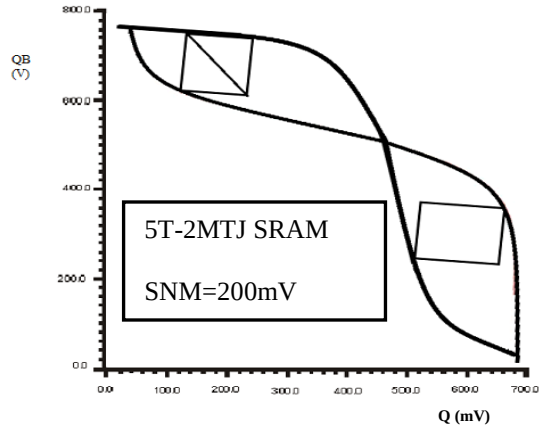


Fig. 6. Test setup for measuring SNM

Above shown schematic shows a trial setup for measuring SNM. After simulating above schematic a butterfly curve is held. The side length of Maximum Square that can be accommodated inside the smaller wing of the butterfly curve represents the SNM of the cell.



SNM influences both the read and write margin, is associated to the threshold voltage of the PMOS and NMOS devices in SRAM cells. Static noise margin (SNM) of the SRAM Cell affected by the cell ratio (CR), supply voltage, and pull up ratio (PR). The value of SNM should be high for stability of SRAM cell and that depends on cell ratio, pull up ratio and supply voltage. Cell ratio shows the ratio across the sizes of the driver transistor to the access transistor for the period of read operation. Pull up ratio makes fixed as the proportion between the sizes of the access transistor to the load transistor for the period of write operation. The SNM of the circuit is determined by the smallest diagonal of the two maximum squares that can he fit across the cross section of the VTC diagrams of the cross-coupled inverters. The SNM of SRAM is calculated and it is 0.184 V, shown in figure 7.

$$SNM = \sqrt{((NMH)^2 + (NML)^2)} \quad (9)$$

$$N_{MH} = V_{OH} - V_{IH} \quad (10)$$

$$N_{ML} = V_{IL} - V_{OL} \quad (11)$$

VII. COMPARISION OF RESULTS

Parameter	***5T–2R SRAM***	***STT-MRAM***
Non-Volatile	No	Yes
Delay	21.54 E-9	20.34 E-9
Total Power	32 E-6	44.6 E-6
SNM	~150	~200mv

VIII. CONCLUSION

In this report, we introduced the characteristics results on the 5T-2MTJ based RAM cell under different facets. MTJ base circuit show one of the most gifted emerging technologies to defeat the high leakage power issue of CMOS circuits and MTJ circuit also provide non volatility, fast random access and infinite endurance. This work carried out on cadence tool, in device design and optimization such as different characteristic parameter profile in 0.7V supply voltage at 45nm technology and gets better result as compared to conventional 5T-2R SRAM. The calculated results indicate that the circuit based on 4T-2MTJ shows non-volatility, power reduction up to 44.6 E-6 and increases the stability in comparison of 5T-2R based SRAM up to ~200mV.

ACKNOWLEDGEMENT

The author would like to thank Institute of Technology and Management, Gwalior for providing the Tools and Technology for the work to be completed.

REFERENCES

1. Mayank Chakraverty, Harish M. Kittur, P. Arun Kumar. First Principle Simulations of Various Magnetic Tunnel Junctions for Applications in Magneto resistive Random Access Memories. IEEE Transactions on Nanotechnology, vol. 12, no. 6: pp. 971-977, Nov. 2013
2. Chika Tanaka, Keiko Abe, Hiroki Noguchi, Kumiko Nomura, Kazutaka Ikegami, Shinobu Fujita. Normally-off type nonvolatile static random access memory with perpendicular spin torque transfer-magnetic random access memory cells and smallest number of transistors. Japanese Journal of Applied Physics, vol. 53, 04EM07, Mar 2014.
3. Zhenyu Sun, Xiuyuan Bi, Hai (Helen) Li, Weng-Fai Wong, Xiaochun Zhu. STT-RAM Cache Hierarchy With Multiretention MTJ Designs. IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, pp. 1281-1293, Jun 2014.
4. Yi Gang, Weisheng Zhao, Jacques-Olivier Klein, Claude Chappert, Pascale Mazoyer. A High-Reliability Low-Power Magnetic Full Adder. IEEE Transactions on Magnetics, vol. 47, no. 11, pp. 4611-4616, Nov. 2011.
5. Leem L, Harris james S. Magnetic coupled spin torque devices for non-volatile logic applications. Journal of applied physics, vol. 105, issue 7, pp. 07D102 - 07D102-3, Apr. 2009
6. Weisheng Zhao, Eric Belhaire, Claude Chappert. Spin Transfer Torque (STT)-MRAM–Based Runtime Reconfiguration FPGA Circuit. ACM Transactions on Embedded Computing Systems, vol. 9, no. 2, article 14, Oct. 2009.
7. Shyam Akashe, Sushil bhushan, Sanjay Sharma. High Density and Low Leakage Current Based 5T SRAM Cell Using 45 nm Technology. Romanian Journal of Information Science and Technology, vol.15, no.2 : 155-168, 2012.
8. Stuart A.Wolf, Jiwei Lu, Stan M.R, Chen E, Treger D. M. The Promise of Nonmagnetic and Spintronics for Future Logic and Universal Memory. Proceedings of the IEEE, vol. 98, no. 12, pp. 2155-2168, Dec. 2010,.
9. Hiwa Mahmoudi, Viktor Sverdlov, Siegfried Selberherr. MTJ-based Implication Logic Gates and Circuit Architecture for Large-Scale Spintronic Stateful Logic Systems. Proceedings of the IEEE conference on the European Solid-State Device research conference, pp. 254-257, Sept. 2012.
10. T. Kawahara, Takemura R, Miura K, Hayakawa J, Ikeda s, Lee Y, "2Mb Spin-Transfer Torque RAM (SPRAM) with Bit-

by-Bit Bidirectional Current Write and Parallelizing-Direction Current Read. Proceeding of the IEEE International Conference on Solid-State Circuits, pp. 480-617, Feb. 2007.

11. Mahadevan Gomathisankaran, Akhilesh Tyagi. WARM SRAM: A Novel Scheme to Reduce Static Leakage Energy in SRAM Arrays. Proceedings to IEEE Computer Society Annual Symposium on VLSI Emerging Trends in VLSI Systems Design (ISVLSI'04), pp. 105-112, Feb. 2004.
12. Aminul Islam, Mohd. Hassan. Variability Analysis of 6T and 7T SRAM Cell in Sub-45nm Technology. IIUM Engineering Journal, vol. 12, no. 1, 2011.
13. Shyam Akashe, Sanjay Sharma. Design of SRAM Cell Based Memory Array in Nano-Scaled Technology. Journal of Computational and Theoretical Nano-science, vol. 10, pp. 1–7, 2013.
14. Shyam Akashe, Sanjay Sharma. High density and low leakage current based SRAM cell using 45 nm technologies. International Journal of Electronics, pp. 1-17, Jun 2012.
15. M. El Baraji, V. Javerliac, W. Guo, G. Prenat, B. Dieny. Dynamic compact model of thermally assisted switching magnetic tunnel junctions. Journal of Applied Physics, vol. 106, pp. 123906(1-6), 2009.
16. J.-B. Kammerer, L. Hebrard, M. Hehn, F. Braun, P. Alnot, A. Schuhl. Compact modeling of a magnetic tunnel junction using VHDL-AMS: computer aided design of a two-axis magnetometer. Proceeding of IEEE Conference on Sensors, vol.3, pp. 1558-1561,
17. Weisheng Zhao, Lionel Torres, Yoann Guillemenet, Luis Vitorio Cargnini, Yahya Lakys, Jacques-Olivier Klein, Dafine Ravelosona, Gilles Sassatelli, Claude Chappert. Design of MRAM based Logic Circuits and its Applications, pp. 431-436, May 2011.
18. Rishubh Garg, Deepak Kumar, Navneet Jindal, Nandita Negi, Chetna Ahuja. Behavioural model of Spin Torque Transfer Magnetic Tunnel Junction, Using Verilog-A. International Journal of Advancements in Research & Technology, vol. 1, pp. 1-7,, Nov. 2012.